

M.Sc. (Phy) Semester - 3 (CBCS) Examination

DEC/JAN. - 2020

Analog and Digital Systems (Elective)

Time: 1:30 Hours

Marks: 42

Instructions:

1. Figure to the right indicate marks.
 2. There are five questions in the question paper.
 3. Answer any three of the following questions.
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Q.1 (14)

- (a) Draw and discuss the functioning of each block in the block diagram of a typical operational amplifier. (7)
- (b) List the ideal op-amp parameters. Define the following electric parameters of an op- Amp : CMRR, (7)
Slew rate, SVRR, and bandwidth.

Q.2 (14)

- (a) Discuss how inverting amplifier with feedback and have more than one inputs can be used as a (7)
summing, scaling, and averaging amplifier.
- (b) write a note on: Zero crossing detector. (7)

Q.3 (14)

- (a) Draw the circuit of the binary half adder. A binary full adder circuit has three inputs: X_n , Y_n and (7)
previous carry C_{n-1} and two outputs SUM and CARRY. Derive canonical Boolean expressions for outputs
and prove that: $SUM = X_n \oplus Y_n \oplus C_{n-1}$. Implement the circuit by using logic gates.
- (b) Design a 4-bit magnitude comparator circuit that compares two binary numbers $A=A_0A_1A_2A_3$ and (7)
 $B=B_0B_1B_2B_3$ and produces three outputs $A=B$, $A>B$, $A<B$. Sketch the circuit neatly.

Q.4 (14)

- (a) Distinguish between buffer and shift register. Write a brief note on the Ring counter. (7)
- (b) Draw the circuit of asynchronous (ripple) MOD-10 counter and explain its operation with counting (7)
sequence and timing diagram.

Q.5 (14)

- (a) Draw the circuit of 8-bit tracking ADC and explain its operation. (7)
- (b) Eight-bit Successive Approximation ADC and its algorithm of the conversion cycle. (7)
